MC Devices®

MCD2006G/S

Transmit ICs with Integrated VCO For FM/FSK Transceiver

General Description

MCD2006G/S is a set of transmit ICs for FM/FSK wireless transceiver intended for use in the VHF band, includes two ICs, MCD2006G and MCD2006S. The ICs contain an integrated VCO, a RF power amplifier, a reference crystal oscillator, and a frequency synthesizer; A completed phase-lock-loop (PLL) is consisted by combining the ICs and on board LPF、inductor and varactors.

The difference between MCD2006G and MCD2006S is S contains a 6-bit ROM，the PLL can be locked at 43 corresponding frequencies when users setup 6-bit ROM logic input shown in fixed logic table on page 14. MCD2006G contains a MCU programmable control interface which is used for setting any targeted division by an external MCU. The PLL provides 3MHz~110MHz carrier frequency. The typical output power of RF amplifier is 3dBm@27MHz with a 50ohm load.

In practical terms MCD2006G must combine with a MCU but MCD2006S can be free of MCU.

Supply voltage range is 2.7 to 4.5 volts. It has been proved that MCD2006G/S can work stably between -40 to +85 degrees.

Typical Applications

- FM transceiver, remote controller
- 27-49M baby monitor, PTT and car radio
- Infrared FM transceiver system

Features

- Operating Frequency：
  MCD2006G: 3MHz~110MHz
  MCD2006S: 43 fixed frequencies shown in the logic table on page 14
- Operating Voltage Range: 2.7~4.5V
  (3.3V Typical)
- Operating Power Consumption:
  19mA@3.3V, 27MHz
- The crystal oscillator supports:
  MCD2006G: 4~25MHz
  MCD2006S:
  4MHz (for 5KHz reference frequency)
  20MHz (for 25KHz reference frequency)
- RF output power: 3dBm@27MHz with 50Ω output impedance.
- Low phase noise: -112dBc/Hz at 10KHz offset, 50Hz loop bandwidth
- TX Modulation: FM/FSK
- RF AMP Output Distortion: <1%
- Modulated Deviation: 5KHz reachable
- Modulated Audio Frequency Range：
  50Hz~30KHz
- Data Rate: 300bps~120kbps
- Package:
  MCD2006G: TSSOP-16
  MCD2006S: SSOP-20L

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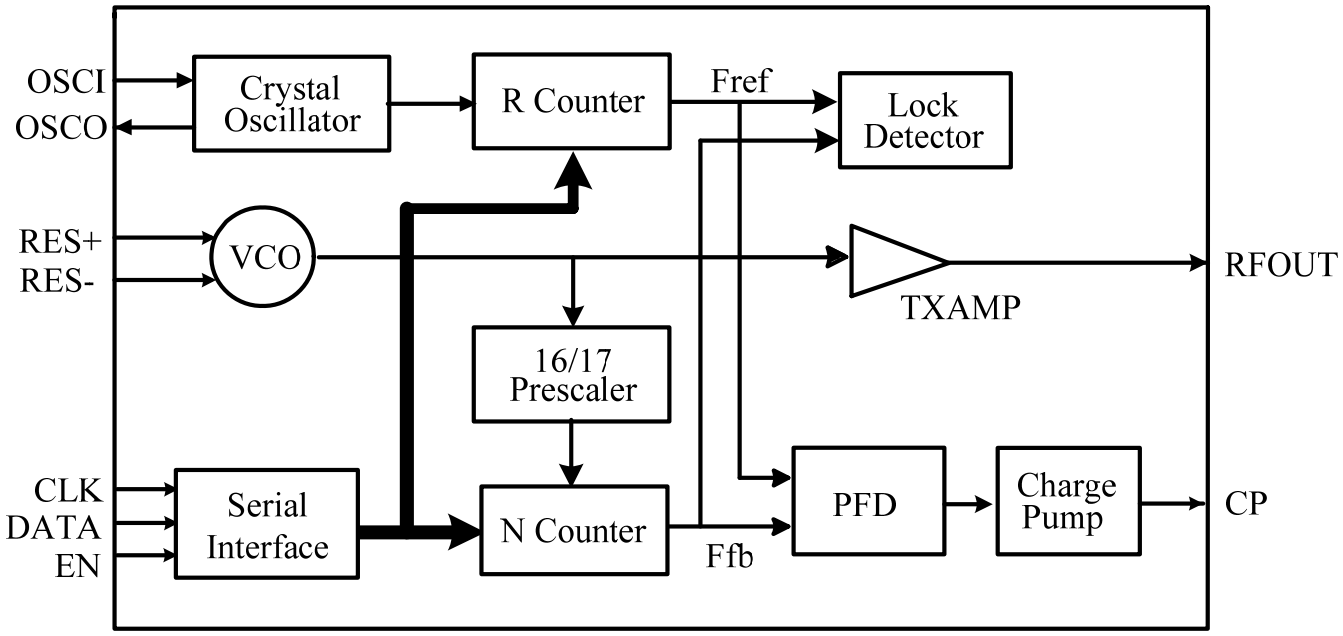
Version History

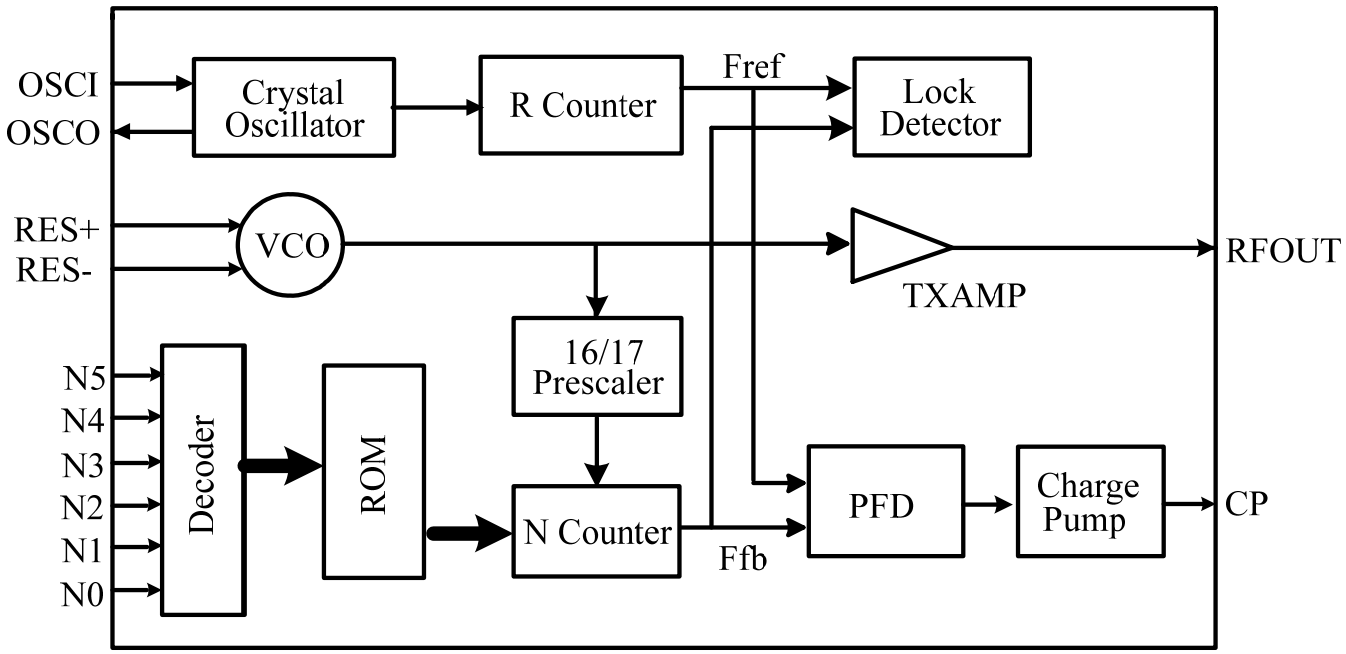
Version	Issued time	Notes
V1.0	Oct. 28, 2006	First English version created
V1.1	Aug. 29, 2008	Add MCD2006S

Function Block Diagram

■ MCD2006G

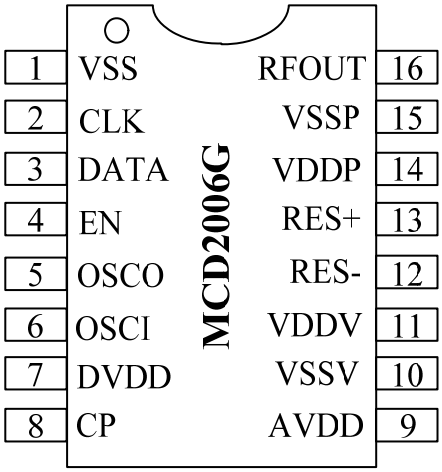


■ MCD2006S



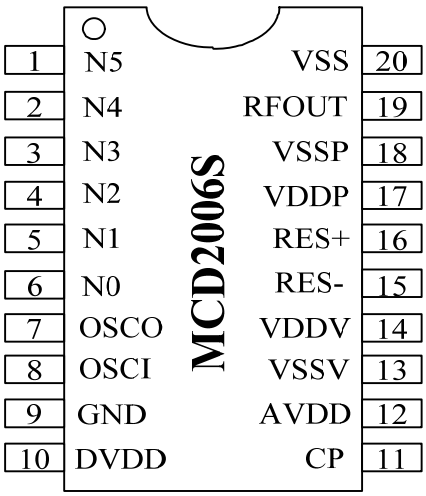
Pin Assignment and Description

▪ MCD2006G



Pin#	Pin Name	I/O	Description
1	VSS	I	Terminal of PLL ground.
2	CLK	I	MCU control clock input. Data are clocked in on the rising edges of the clock.
3	DATA	I	MCU serial data input. LSB are sent in first and last two bits are group code.
4	EN	I	MCU control enable input. When EN is high level, the data saved in shift register is loaded into appropriate counter (determined by group code).
5	OSCO	O	Output terminal of crystal oscillator. This pin is connected to the crystal when the reference frequency is generated by the crystal oscillator.
6	OSCI	I	Input terminal of crystal oscillator. The pin is connected to the crystal when the reference frequency is generated by the local oscillator. It also can be driven by an external clock.
7	DVDD	I	Digital circuit power supply (2.7-4.5V).
8	CP	O	Output terminal of charge pump. Connecting to the loop filter to drive the voltage control input of the VCO.
9	AVDD	I	Analogue circuit power supply (2.7-4.5V).
10	VSSV	I	Terminal of VCO ground.
11	VDDV	I	VCO circuit power supply (2.7-4.5V).
12	RES-	I	The RES pins are used to supply DC voltage to the VCO, as well as to tune the centre frequency of the VCO. Equal value capacitors should be connected to this pin and pin 13.
13	RES+	I	Same as pin12.
14	VDDP	I	RF power amplifier circuit power supply (2.7-4.5V).
15	VSSP	I	Terminal of RF power amplifier ground.
16	RFOUT	O	RF output pin. Typical output power is 3dBm@27MHz with 50Ω output impedance.

■ MCD2006S



Pin#	Pin Name	I/O	Description
1~6	N5~N0	I	6^{th}~1^{st} ROM control bit. When the pin floats, the logic level is low, when the pin is connected to VDD, the logic level is high.
7	OSCO	O	Output terminal of crystal oscillator. This pin is connected to the crystal when the reference frequency is generated by the crystal oscillator.
8	OSCI	I	Input terminal of crystal oscillator. The pin is connected to the crystal when the reference frequency is generated by the local oscillator. It also can be driven by an external clock.
9	GND	I	Terminal of ground.
10	DVDD	I	Digital circuit power supply (2.7-4.5V).
11	CP	O	Output terminal of charge pump. Connecting to the loop filter to drive the voltage control input of the VCO.
12	AVDD	I	Analogue circuit power supply (2.7-4.5V).
13	VSSV	I	Terminal of VCO ground.
14	VDDV	I	VCO circuit power supply (2.7-4.5V).
15	RES-	I	The RES pins are used to supply DC voltage to the VCO, as well as to tune the centre frequency of the VCO. Equal value capacitors should be connected to this pin and pin 16.
16	RES+	I	Same as pin15.
17	VDDP	I	RF power amplifier circuit power supply (2.7-4.5V).
18	VSSP	I	Terminal of RF power amplifier ground.
19	RFOUT	O	RF output pin. Typical output power is 4dBm@49MHz with 50Ω output impedance.
20	VSS	I	Terminal of analogue circuit ground.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typical	Max	
Power Supply Voltage	VDD	2.7	3.3	4.5	V
Operating Temperature	T_A	-40	27	+85	℃

Electrical Characteristics (VDD=3.3V, -40℃≤T_A≤+85℃； except as specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
General Characteristics							
F_{OUT}	Operating Frequency	MCD2006G		3	27	110	MHz
		MCD2006S(see the appendix)		3.2		49.950	
F_{OSC}	Crystal Frequency	MCD2006G		4		25	MHz
		MCD2006S	5KHz reference frequency	/	4	/	
			25KHz reference frequency	/	20	/	
F_{PD}	Phase Detector Frequency	MCD2006G		set by users			KHz
		MCD2006S	4MHz crystal	/	5	/	
			20MHz crystal	/	25	/	
V_{IH}	High-Level Input Voltage			0.8		1	VDD
V_{IL}	Low-Level Input Voltage			0.1		0.3	V
I_{DD}	Power Consumption	F_{OUT} =27MHz			19		mA
		F_{OUT} =49MHz			17		
		F_{OUT} =100MHz			18		
I_{CP}	Charge Pump Current				±800		uA
RF							
V_{CP}	VCO Control Voltage			0.5		VDD-1.0	V
P_{OUT}	Output Power	F_{OUT} =27MHz			3		dBm
		F_{OUT} =49MHz			4		
		F_{OUT} =100MHz			5		
HS_{OUT}	Harmonic Suppression (The matching network is shown in application circuit)	F_{OUT} =27MHz	2nd Harmonic 50Ω Load		-54		dBm
			3rd Harmonic 50Ω Load		-53		
		F_{OUT} =49MHz	2nd Harmonic 50Ω Load		-57		
			3rd Harmonic 50Ω Load		-59		
		F_{OUT} =100MHz	2nd Harmonic 50Ω Load		-53		
			3rd Harmonic 50Ω Load		-54		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
K_{VCO}	Fine Tuning Sensitivity (varactor ISV149)	F_{OUT}=27MHz			3		MHz/V
		F_{OUT}=49MHz			900		KHz/V
Z_{OUT}	Output Impedance				50		Ω
PN_{OUT}	Phase Noise	F_{OUT} =27MHz	1KHz offset		-88		dBc/Hz
			10KHz offset		-112		
			100KHz offset		-124		
		F_{OUT} =49MHz	1KHz offset		-77		
			10KHz offset		-106		
			100KHz offset		-116		
		F_{OUT} =100MHz	1KHz offset		-77		
			10KHz offset		-104		
			100KHz offset		-124		
Modulation (TX)							
S_{AF}	Audio Frequency Range			50		30K	Hz
S_{DR}	Data Rate			300		120K	bps
D_{EV}	FM Deviation (1SV149, 300~3K BPF)	F_{OUT} =27MHz		0.035		0.045	KHz
		F_{OUT} =49MHz		0.03		0.04	
F_{MD}	Modulated Deviation	26mV amplitude, F_{OUT} =27MHz			±3		KHz
		23mV amplitude, F_{OUT} =49MHz			±3		
SNR	S/N (3KHz modulation-port character,300~3KBPF)	F_{OUT} =27MHz			44		dB
		F_{OUT} =49MHz			44		
DIS	Audio Distortion	demodulated AF				1.0	%

1. Function Description

1.1 ROM mode

MCD2006S works at ROM mode only. The 6-bit input data N0-N5 is decoded to 64 control lines by X-Y crossed combination. The 64 lines correspond to 64 18-bit parallel outputs which are sent to prescaler and counters. Channels 22~32、43~48、62~64 are reserved for IC design test only.

64 channels are partitioned to 4 groups, which are shown in appendix in detailed. Users set the logic level of N0~N5 according to the logic table, PLL will lock at the corresponding frequency.

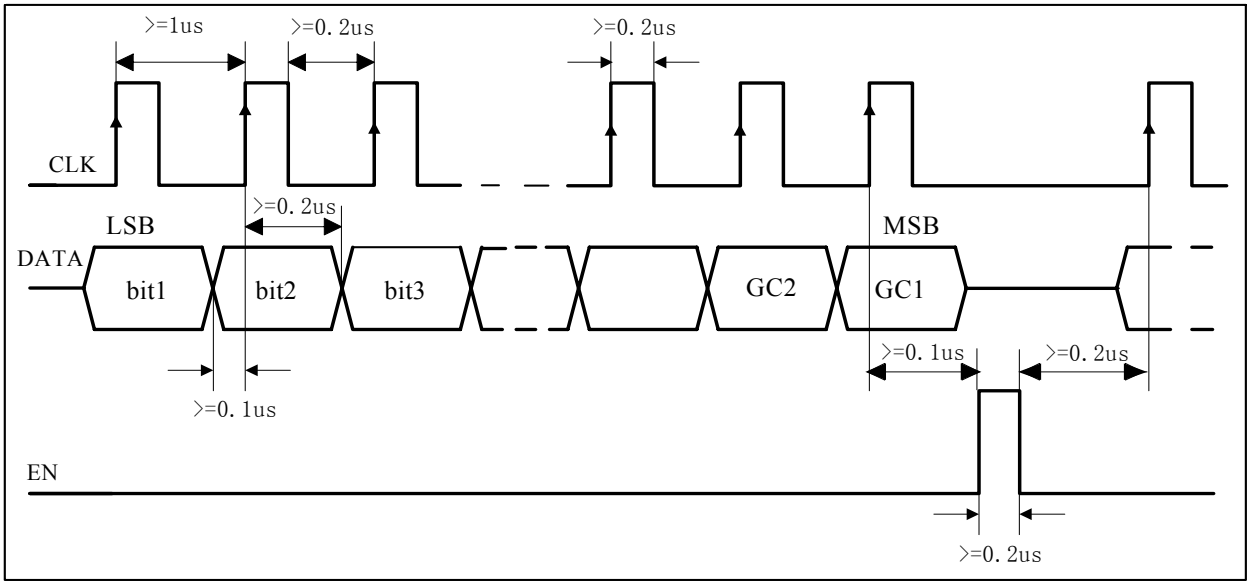
The frequencies in Group A and B are set for IR FM transmitter whose reference frequency is chosen as 25KHz. While frequencies in Group C and D are set for baby monitor system whose reference frequency is chosen as 5KHz.

1.2 MCU mode

MCD2006G works at MCU mode only. The CLK, DATA, and EN pins are used for serial data interface. Binary serial data enter via the DATA pin, go through serial-to-parallel interface to configure reference counter and channel N counter separately according to the group code.

Data shift in shift register at the rising edge of the CLK signal. Firstly LSB data are shifted in, and then the last two bits (group code) decode the internal register address. At the rising edge of EN signal, shifted data are loaded into one of the two appropriate counters.

The input CLK, DATA and EN timing should follow drawing diagram.



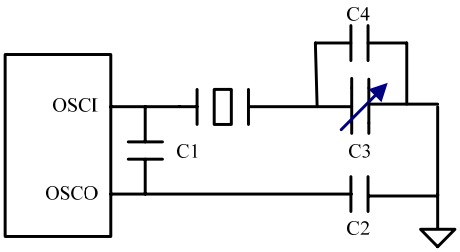
Notes: (1) LSB data are shifted in first.
(2) When power up, usually R counter is configured before N counter.

Group code assignment:

GROUP CODE		LOCATION
GC1 (MSB)	GC2 (LSB)	
0	0	Control Latch(test purpose only)
1	0	Channel N counter
1	1	Reference counter

1.3 Reference Oscillator

The reference frequency for PLL is obtained by applying an external crystal and a few capacitors. External capacitors C1 to C4 are required to set the proper crystal's load capacitance and oscillation frequency. MCD2006S has to apply 4MHz crystal for getting a 5KHz reference frequency or 20MHz crystal for getting a 25KHz reference frequency.



1.4 Reference Divider (R counter)

The reference divider provides reference frequency for PFD (Phase Frequency Detector). It includes a fixed 1/2 divider and a 10-bit programmable divider. The 10-bit divider can program the division ratio between 3 and 1023. Due to the fixed 1/2 divider, the total division ratio for reference divider will range from 6 to 2046.

The division ratio of MCD2006S is fixed at 800 internally, so a 4MHz crystal is a must to create 5KHz reference frequency, and a 20MHz crystal is a must to create 25KHz reference frequency.

The division ratio of MCD2006G is set by an external MCU. See the programming description at Section 2 for details.

1.5 Feedback Divider (N counter)

The channel N **c**ounter is clocked by the RF signal generated by VCO. The N counter consists of a 4-bit swallow counter with a division ratio 0<A<15 and a 12-bit pulse counter with a division ratio 3<B<4095. In conjunction with the 16/17 prescaler, the total division ratio can range from 48 to 65535 on the feedback channel. For the proper operation of the prescaler, the pulse counter division ratio B should be always equal to or greater than the swallow counter division ratio A.

The division ratio of MCD2006S is set by ROM. Users simply set the input level of N0-N5 following the logic table, the internal decoder and ROM will read appropriate division ratio and send it to the N counter. There is no calculation and configuration requirement for the users.

The division ratio of MCD2006G is determined by an external MCU. See the programming description at Section 2 for details.

1.6 Prescaler

The prescaler of MCD2006 consists of a pre-amplifier, and a CMOS 16/17 dual modulus divider. The prescaler offers clock to the subsequent CMOS N counter.

1.7 Phase/Frequency Detector (PFD)

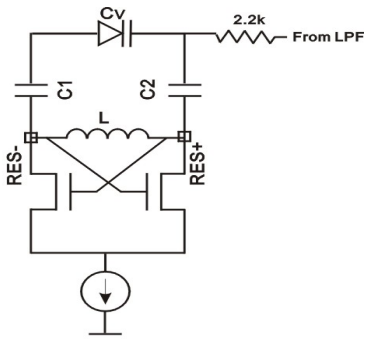
PFD compares frequency and phase of two inputs from reference counter and N counter, outputs control logic to charge pump. The PFD receives a feedback signal from charge pump in order to eliminate dead zone.

1.8 Charge Pump

The charge pump pumps **u**p current to an external loop filter, or pumps down from the filter according to the polarity control of its PFD outputs. The loop filter converts the charge into VCO's control voltage. The charge pump steers the charge pump output CP to VDD (pump-up) or GND (pump-down). Under the locked condition, CP is primarily in a TRI-STATE mode with small corrections. The charge pump current magnitude is ±800uA.

1.9 VCO

VCO is a tuned differential amplifier with the gate and drain cross coupled to provide positive feedback and a 360° phase shift (shown in the following picture). It is comprised an external inductor, two capacitors, two varactors and internal circuits. The users need to select appropriate inductors for the desired frequency of operation. The output of the VCO is applied to the TXAMP and buffered to prescaler circuit, where it is divided down and compared to the reference frequency.



The setup of the VCO can be summarized as follows. Firstly, open the loop, build up an oscillation (as shown in above picture). Two capacitors connected at pin RES- and RES+ are recommended as 100~120pF (when loop locked at 49MHz). The inductor connected between pin RES- and RES+ need to be calculated according to following equation.

$$L = (\frac{1}{2\pi f})^2 \frac{1}{C}$$

C = C1 or C2 //Cv

Cv: varactor capacitance corresponding to applied LPF voltage, check varactor datasheet.

In above equation, the value of C is the amount of capacitance presented by varactors, capacitors and parasitic. For rough calculation, the parasitic value can be ignored.

Define the VCO frequency as the lowest frequency F1 when setting the negative end of Cv to 0V, define the VCO frequency as the highest frequency F2 when setting the negative end of Cv to VDD. F1 and F2 determine VCO frequency range. Users need to guarantee the targeted frequency is within the range, staying at middle is recommended.

Secondly, add LPF in to become a close loop (shown in application circuit). At this moment, the voltage level of the negative end of Cv is controlled by the added LPF, when this voltage fixes at a stable level, the loop locks. The voltage level of LPF should be within the control voltage range of VCO.

1.10 TXAMP

The RF amplifier is an output stage. The amplifier of the chip is capable of providing 4dBm @49MHz output power to a 50ohm load while operating at 3.3V power supply.

2. Programming Description

2.1 Reference counter

The reference counter provides reference frequency for PLL. It includes a fixed 1/2 divider and a 10-bit programmable divider. The 10-bit divider can program the division ratio between 3 and 1023. Due to the fixed 1/2 divider, the total division ratio for reference divider can be set from 6 to 2046.

LSB Configuration word MSB

R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	GC2=1	GC1=1

Division ratio of the programmable 10bit R counter:

Division ratio (R)	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	1	0	0
●	●	●	●	●	●	●	●	●	●	●
1023	1	1	1	1	1	1	1	1	1	1

$R = R1x2^0 + R2x2^1 + \ldots + R10x2^9$ (R≥3)

The total division ratio range: 6 to 2046.

2.2 Channel N counter

This programmable counter is composed of a 4-bit swallow counter and a 12-bit pulse counter, in conjunction with the 16/17 prescaler to provide division ratio range from 48 to 65535.

LSB configuration word MSB

N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	GC2=0	GC1=1

|------swallow counter------|----------pulse counter----------|------group code------|

Swallow counter division ratio (A)

Division ratio (A)	N4	N3	N2	N1
0	0	0	0	0
1	0	0	0	1
●	●	●	●	●
15	1	1	1	1

$A = N1x2^0 + N2x2^1 + \ldots + N4x2^3$

Division ratio range: 0 to 15

Pulse counter division ratio (B)

Division ratio (B)	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
●	●	●	●	●	●	●	●	●	●	●	●	●
4095	1	1	1	1	1	1	1	1	1	1	1	1

$B = N5x2^0 + N6x2^1 + \ldots + N16x2^{11}$

Division ratio range: 3 to 4095 (B≥A)

Total division ratio of programmable N counter:

N = 16 * B + A (B≥A)

Division ratio range: 48 to 65535

3. Configuration Examples

Example A: To get a 5KHz reference frequency from a 4MHz crystal

- Total division ratio 2R = 4MHz÷5KHz = 800
- Programmable division ratio R = 800÷2 = 400
- Binary format (10bit) R=0110010000
- Group code "11"
- Configuration word(12bit) "110110010000"

LSB(first in) → MSB

0	0	0	0	1	0	0	1	1	0	1	1

Example B: To synthesize a 40.665MHz frequency from a 5KHz reference frequency

- Reference frequency 5KHz (see Example A)
- Total division ratio 16*B + A = 40.665MHz÷5KHz = 8133
- Pulse counter division ratio B = Int (8133÷16) = 508
- Binary format (12-bit) B = 000111111100
- Swallow counter division ratio A = 8133 - 16*508 = 5
- Binary format (4bit) A=0101
- Group code "10"
- Configuration word(18bit) "100001111111000101"

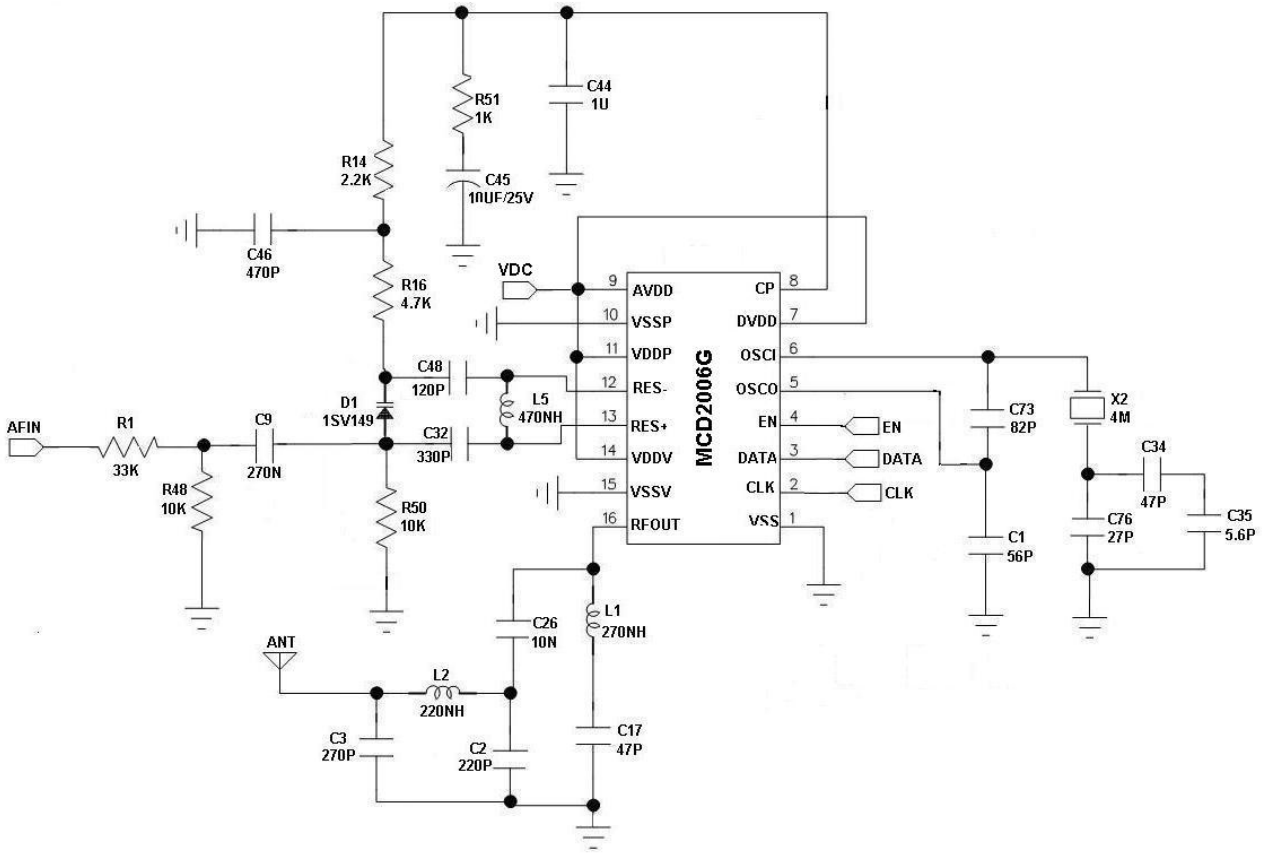
LSB(first in) → MSB

1	0	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	1

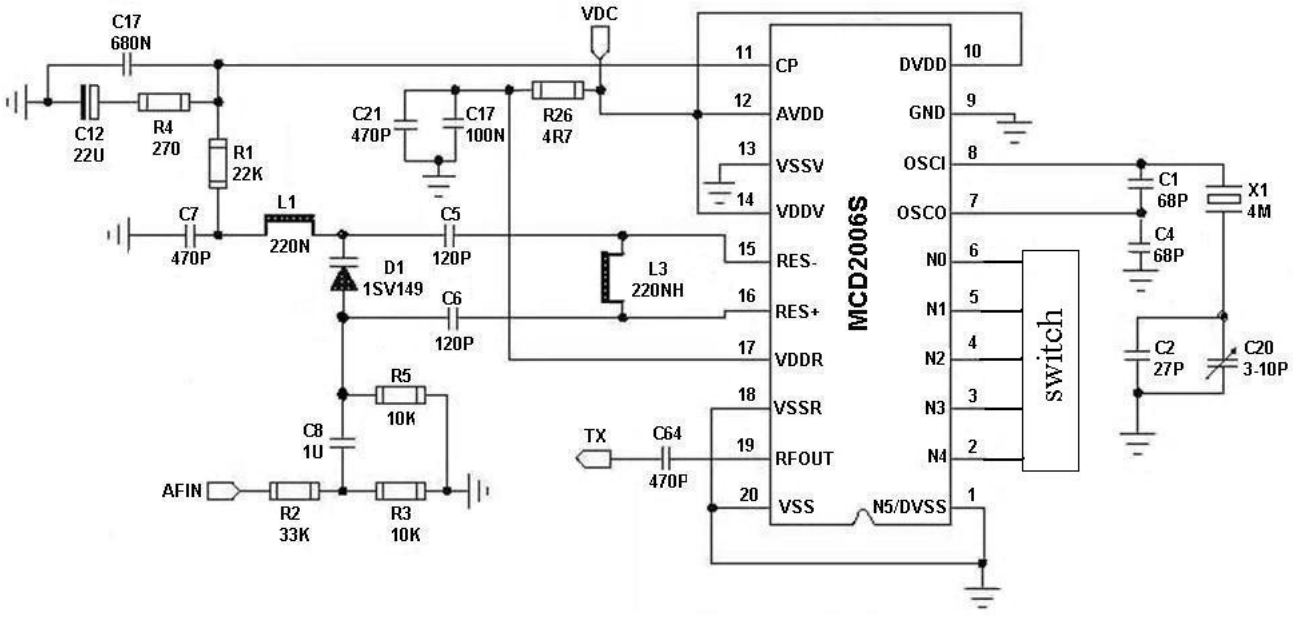
4. Typical Application Circuit

Reference Schematic

■ For MCD2006G 27MHz with 50Ω output impedance matching:

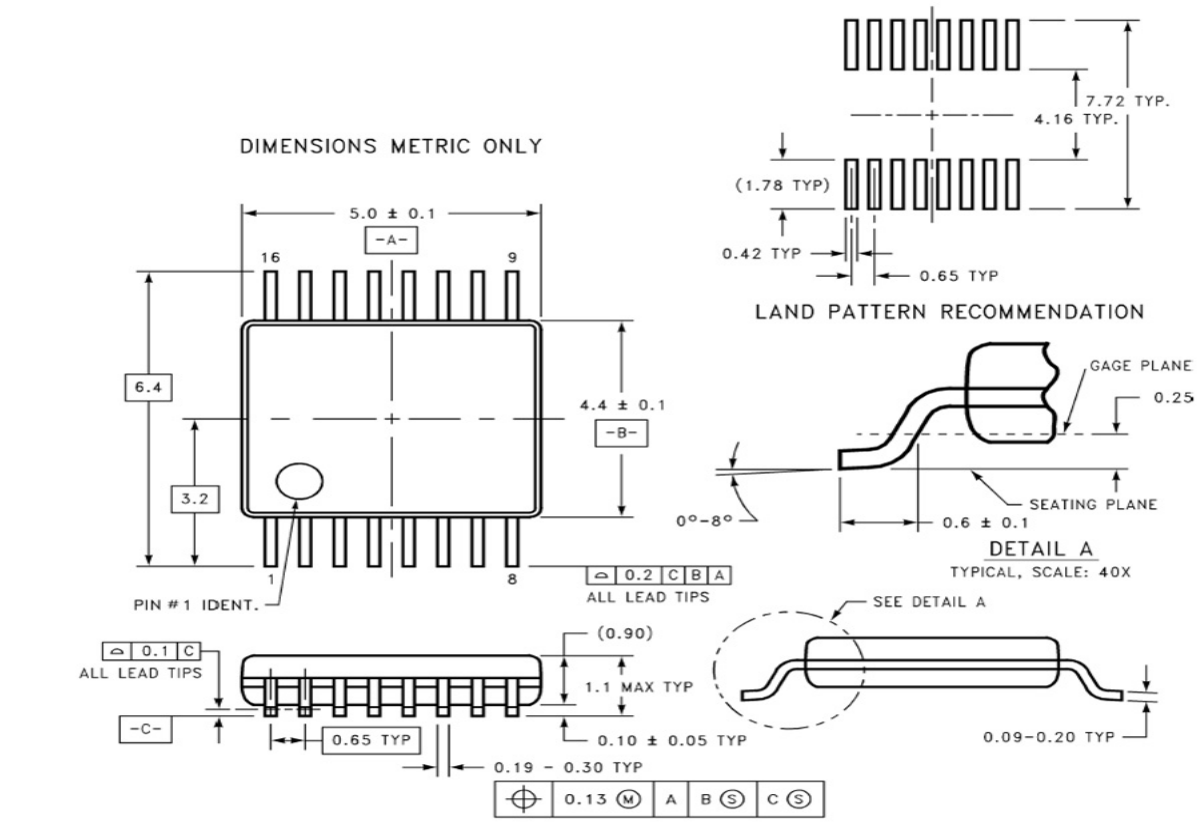


■ For MCD2006S 49MHz with 50Ω output impedance matching:



5. Package Dimensions

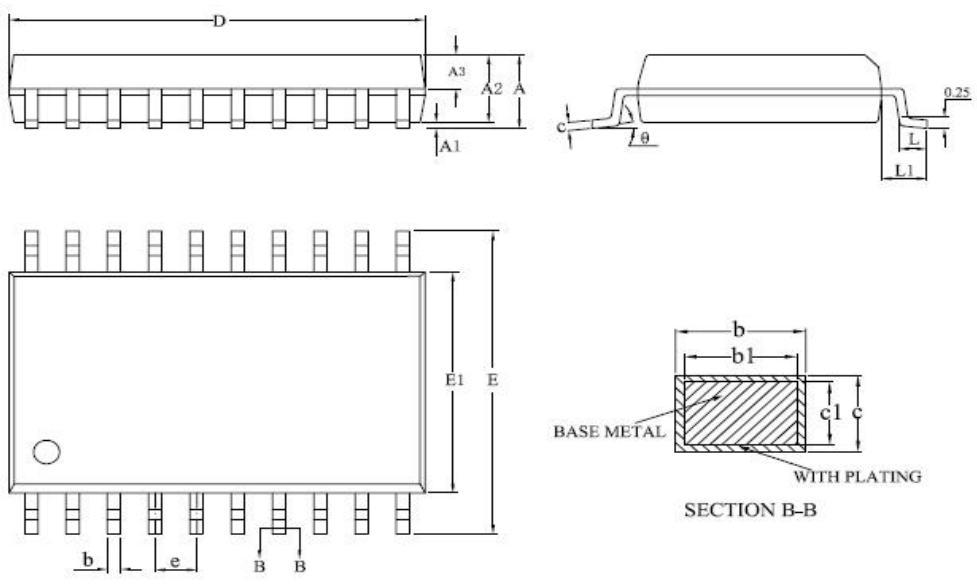
■ TSSOP-16



Dimensions are in millimeters.

16-Pin TSSOP Package

■ SSOP-20L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.85
A1	0.05	—	0.25
A2	1.40	1.50	1.60
A3	0.62	0.67	0.72
b	0.29	—	0.37
b1	0.28	0.30	0.33
c	0.15	—	0.20
c1	0.14	0.15	0.16
D	7.00	7.20	7.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
e	0.65BSC		
L	0.75	—	1.05
L1	1.25BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	145*169		

Appendix: MCD2006S ROM logic table

Note: The background letters A~D denote channel group

No	N5	N4	N3	N2	N1	N0	Fvco (MHz)	No	N5	N4	N3	N2	N1	N0	Fvco (MHz)
1	0	0	0	0	0	0	3.2	17	0	1	0	0	0	0	7.0
2			0	0	0	1	3.4	18			0	0	0	1	7.2
3			0	0	1	0	3.6	19			0	0	1	0	7.5
4			0	0	1	1	3.8	20			0	0	1	1	7.8
5			0	1	0	0	4.0	21			0	1	0	0	8.0
6			0	1	0	1	4.2	22			0	1	0	1	Test
7			0	1	1	0	4.5	23			0	1	1	0	Test
8			0	1	1	1	4.8	24			0	1	1	1	Test
9			1	0	0	0	5.0	25			1	0	0	0	Test
10			1	0	0	1	5.2	26			1	0	0	1	Test
11			1	0	1	0	5.5	27			1	0	1	0	Test
12			1	0	1	1	5.8	28			1	0	1	1	Test
13			1	1	0	0	6.0	29			1	1	0	0	Test
14			1	1	0	1	6.2	30			1	1	0	1	Test
15			1	1	1	0	6.5	31			1	1	1	0	Test
16			1	1	1	1	6.8	32			1	1	1	1	Test
33	1	0	0	0	0	0	40.660	49	1	1	0	0	0	0	49.860
34			0	0	0	1	40.665	50			0	0	0	1	49.830
35			0	0	1	0	40.670	51			0	0	1	0	49.840
36			0	0	1	1	40.675	52			0	0	1	1	49.890
37			0	1	0	0	40.680	53			0	1	0	0	49.850
38			0	1	0	1	40.685	54			0	1	0	1	49.880
39			0	1	1	0	40.690	55			0	1	1	0	49.950
40			0	1	1	1	-	56			0	1	1	1	49.920
41			1	0	0	0	40.700	57			1	0	0	0	49.900
42			1	0	0	1	40.695	58			1	0	0	1	49.870
43			1	0	1	0	Test	59			1	0	1	0	49.930
44			1	0	1	1	Test	60			1	0	1	1	49.940
45			1	1	0	0	Test	61			1	1	0	0	49.910
46			1	1	0	1	Test	62			1	1	0	1	Test
47			1	1	1	0	Test	63			1	1	1	0	Test
48			1	1	1	1	Test	64			1	1	1	1	Test

Important Notice

MC Devices reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to MC Devices' terms and conditions of sale supplied at the time of order acknowledgment.

MC Devices warrants performance of its products to the specifications applicable at the time of sale in accordance with MC Devices' standard warranty. Testing and other quality control techniques are also support this warranty.

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